Attorney Docket No.: 015114-064000US
Client Reference No.: A863

# PATENT APPLICATION

# HYBRID PHASE/DELAY LOCKED LOOP CIRCUITS AND METHODS

Inventor: Bruce Pedersen, a citizen of The United States, residing at
325 Bluefield Dr.
San Jose, CA 95136

Assignee: Altera Corporation
101 Innovation Drive
San Jose, CA, 95134

Entity: Large

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400

# HYBRID PHASE/DELAY LOCKED LOOP CIRCUITS AND METHODS

## BACKGROUND OF THE INVENTION

**[0001]** The present invention relates to the field of electronic circuits, and more particularly, to circuits that include many of the features and advantages of delay locked loops and phase locked loops.

**[0002]** A phase-locked loop (PLL) is a circuit that measures variations in the phase of an input signal. A PLL operates by adjusting the phase of a periodic signal generated by an oscillator. The PLL aligns the phase of the oscillator signal with the phase of the input signal. Variations in the phase of the oscillator signal track variations in the phase of the input signal. When the phase of the oscillator signal and the input signal are perfectly aligned, the two signals are said to be in lock. Typically, a PLL has several programmable frequency dividers that multiply or divide down the frequency of the input signal.

**[0003]** A delay-locked loop (DLL) is a circuit that delays an input signal by an adjustable time period. A DLL generates an output signal using an adjustable delay circuit. The output signal is a time delayed version of the input signal. The DLL automatically adjusts the time delay between the input and output signals to equal approximately one period of the input signal.

**[0004]** Many types of integrated circuits can use either a PLL or a DLL to perform a desired function. For example, programmable logic devices (PLDs) use either a PLL or a DLL to generate on-chip clock signals. A DLL or a PLL circuit can be used to offset the phase of an off-chip clock signal in order to improve either the setup time or the clock-to-output delay of input/output signals (e.g., by anticipating the next clock edge).

**[0005]** Both DLLs and PLLs have advantages and disadvantages. PLLs can be used to generate a stable signal when the input signal has a large jitter. PLLs can also be used to multiply and divide down a clock signal by large integer or by rational ratios.

**[0006]** DLLs have less jitter and drift than PLLs when the incoming clock already has a low jitter. DLLs can also lock and resynchronize more quickly to changes in the phase of the incoming clock signal, and have more robust stability constraints. However, DLLs cannot be easily used to divide or multiply the frequency of the incoming clock signal.

[0007] Because some applications can use either a PLL or a DLL to perform a particular function, a design engineer must consider the trade-offs between the advantages and disadvantages of using these two types of circuits. It would therefore be desirable to provide a circuit that can align the phase of an output signal with the phase of an input signal and that has the advantages of both a DLL and a PLL.

## BRIEF SUMMARY OF THE INVENTION

[0008] The present invention provides circuits and methods for adjusting the phase of a periodic clock signal using a hybrid PLL/DLL circuit. A hybrid PLL/DLL circuit of the present invention functions as a phase locked loop (PLL) in a first state of operation and as a delay locked loop (DLL) in a second state of operation.

[0009] A hybrid PLL/DLL circuit aligns the phase of a periodic delay signal with an input clock signal. An adjustable delay circuit generates the delay signal. A phase detector compares the input clock signal to the delay signal to generate a phase detection signal. The adjustable delay circuit adjusts the phase of the delay signal in response to the phase detection signal.

[0010] A multiplexer couples the delay signal back to the input of the adjustable delay circuit using a feedback loop in the first state of operation. After a period of time, the multiplexer couples the input clock signal to the input of the adjustable delay circuit in the second state of operation.

[0011] Circuits of the present invention have many of the advantages of both phase locked loops and delays locked loops. For example, circuits of the present invention can adjust the phase of the output signal to align instantaneously with changes in the phase of the input signal in the second state of operation.

[0012] Also, the jitter and the drift of the output signal is matched to the jitter and drift of the input signal during the second state of operation. In addition, circuits of the present invention can adjust the frequency of the output signal to match changes in the frequency of the input signal more quickly than standard PLL circuits. Further, the frequency of the output signal can be divided by a ratio of N/M using frequency dividers.

[0013] Other objects, features, and advantages of the present invention will become apparent upon consideration of the following detailed description and the accompanying drawings, in which like reference designations represent like features throughout the figures.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Figure 1 is block diagram of a delay locked loop circuit;

[0015] Figure 2 is a block diagram of a phase locked loop circuit;

[0016] Figure 3 is a block diagram of an embodiment of a hybrid PLL/DLL circuit according to the present invention;

[0017] Figure 4 is a timing diagram that illustrates examples of signals generated by the circuit if Figure 3 in hybrid PLL/DLL mode;

[0018] Figure 5 is a timing diagram that illustrates examples of signals generated by the circuit if Figure 3 in PLL mode;

[0019] Figure 6 is a simplified block diagram of a programmable logic device that can implement embodiments of the present invention; and

[0020] Figure 7 is a block diagram of an electronic system that can implement embodiments of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

[0021] Figure 1 illustrates an embodiment of a delay locked loop (DLL) circuit 100. DLL 100 includes a phase detector circuit 101 and an adjustable delay circuit 102. Adjustable delay circuit 102 in DLL 100 receives clock signal VIN as an input signal and generates clock signal VOUT as an output signal. Adjustable delay circuit 102 delays VIN to generate VOUT. Thus, VOUT is a delayed and inverted version of VIN. VOUT can be delayed with respect to VIN, for example, by one-half of a period of VIN. Adjustable delay circuit 102 can include, for example, a plurality of buffers (e.g., inverters) coupled together in series between VIN and VOUT.

[0022] Phase detector circuit 101 include a phase comparator. The phase comparator compares the phase of input signal VIN with the phase of output signal VOUT. Phase detector 101 transmits a phase detection signal to adjustable delay 102 that indicates if VIN

and VOUT are out of phase and by how much they are out of phase. In response to the phase detection signal, adjustable delay circuit 102 controls the delay between VIN and VOUT.

**[0023]** For example, if phase detector 101 determines that corresponding rising edges of VIN and VOUT are offset by more than one period, the phase detection signal causes adjustable delay circuit 102 to decrease the phase of VOUT. Adjustable delay circuit 102 can decrease the phase of VOUT by decreasing the delay introduced between signals VIN and VOUT. Delay circuit 102 continues to decrease the phase of VOUT until the phase detection signal indicates that the phases of VIN and VOUT are offset by one period of VIN.

**[0024]** If phase detector 101 determines that the phases of VIN and VOUT are offset by less than one period, the phase detection signal causes adjustable delay circuit 102 to increase the phase of VOUT. Delay circuit 102 can increase the phase of VOUT by increasing the delay introduced between signals VIN and VOUT. Delay circuit 102 continues to increase the phase of VOUT until the phase detection signal indicates that the phases of VIN and VOUT are offset by one period of VIN.

**[0025]** Adjustable delay circuit 102 can, for example, include a capacitor coupled between two of the buffers in the delay circuit. Delay circuit 102 can cause the charge and/or discharge rate of the capacitor to vary in response to the phase detection signal.

**[0026]** Figure 2 illustrates an embodiment of a phase locked loop (PLL) circuit 200. PLL 200 includes a phase detector 201, a voltage controlled oscillator (VCO) 202, and frequency dividers 203-204. PLL 200 also receives a clock input signal VIN and generates a clock output signal VOUT. VCO 202 generates a periodic clock signal VOS as shown in Figure 2.

**[0027]** Frequency divider 203 divides the frequency of VOS by a first whole number N to generate a signal VN. The frequency of VN is 1/N times the frequency of VOS. Frequency divider 204 divides the frequency of VOS by a second whole number M to generate output signal VOUT. The frequency of VOUT is N/M times the frequency of VIN.

**[0028]** The frequency of VOS is typically much larger than the frequency of input signal VIN. Frequency divider 203 divides the frequency of VOS to generate a signal VN with a frequency that is closer to the frequency of VIN.

**[0029]** Phase detector 201 includes a comparator that compares the phases of input signal VIN with signal VN. Phase detector 201 transmits a phase detection signal to VCO 202 that indicates the difference between the phases of VIN and VN. Phase detector 201 can also

include a charge pump circuit and/or a level shift circuit that increase the voltage of the comparator output signal. Further details of functional and structural embodiments of a phase locked loop circuit that can be incorporated into hybrid PLL/DLL circuits of the present invention are discussed in detail in commonly assigned U.S. Patent 6,369,624, filed November 2, 1999, to Wang et al., which is incorporated by reference herein.

**[0030]** The phase detection signal is transmitted to an input of VCO 202. VCO 202 includes an adjustable delay circuit 210. Adjustable delay circuit 210 controls when the edges of clock signal VOS occur. Adjustable delay circuit 210 can, for example, include an odd number of inverting buffers coupled together in series. An alternating signal passes through the buffers. The output of one of the buffers generates periodic clock signal VOS. Delay circuit 210 is shown with an inversion at its output to indicate that delay circuit 210 inverts VIN to generate VOS.

**[0031]** VCO 202 can include, for example, a ring oscillator. A ring oscillator includes an odd number of inverting buffer circuits coupled to a feedback loop. Feedback loop 212 shown in Figure 2 is the feedback loop. Feedback loop 212 is coupled to an input and an output of adjustable delay circuit 210. Feedback loop 212 couples the buffers in delay circuit 210 together into a ring oscillator.

**[0032]** Adjustable delay circuit 210 controls the phase of VOS in response to the phase detection signal. For example, adjustable delay circuit 210 can include a capacitor coupled between a chain of buffers coupled together in delay circuit 210. The phase detection signal from detector 201 controls the charge and/or discharge rate of the capacitor to adjust the phase of VOS.

**[0033]** When VIN and VN are out of phase, the phase detection signal causes adjustable delay circuit 210 to change the phase of VOS so that VN aligns with VIN. When VN and VIN are aligned, VCO 202 maintains the phase of VOS constant in response to the phase detection signal. Further details of the operation of an exemplary phase detector circuit are discussed in U.S. Patent 6,369,624 mentioned above.

**[0034]** Figure 3 illustrates an embodiment of a hybrid PLL/DLL circuit 300 of the present invention. Circuit 300 includes circuit 302, phase detector circuit 201, frequency dividers 203-204, AND gate 310, memory circuit 320, and edge detector circuit 315. Circuit 302 includes a multiplexer 305, feedback loop 312, and adjustable delay circuit 210 that are coupled as shown in Figure 3.

[0035] Hybrid PLL/DLL circuit 300 functions in two different states of operation. In the first state of operation, circuit 300 attempts to align the phase of input clock signal VIN with an internally generated clock signal. Circuit 302 is configured as a voltage control oscillator (VCO) in the first state of operation to generate a delay clock signal VT.

[0036] During the first state of operation, memory bit 320 is set HIGH to pass the output signal of edge detector 315 to the select input of multiplexer 305 as VSEL. Edge detector 315 can be part of divider circuit 203.

[0037] The output signal of edge detector 315 (and VSEL) go HIGH one-half of a VT cycle before a rising edge of VN (see, e.g., Figure 4). The output signal of edge detector 315 (and VSEL) go LOW one-half of a VT cycle after the rising edge of VN. The output signal of edge detector 315 and VSEL are HIGH for one period of VT.

[0038] Edge detector 315 can be, for example, a counter circuit. The counter circuit can be part of divider 203. According to this embodiment of the present invention, the counter circuit counts N – 1 rising edges of VT. After the counter circuit detects N – 1 rising edges of VT, the counter circuit causes VSEL to go HIGH one-half of a VT clock cycle before a rising edge of VN. After VSEL goes HIGH, the counter circuit resets its count value to zero. VSEL goes LOW after one period of VT. After VSEL goes LOW, the counter circuit begins to count the rising edges of VT again.

[0039] When the output signal of edge detector 315 is LOW (and memory bit 320 is HIGH), VSEL is LOW, causing multiplexer 305 to couple feedback loop 312 to an input of adjustable delay circuit 210. Adjustable delay circuit 210 can comprise an odd number of inverting buffers, as discussed above. When feedback loop 312 is coupled around adjustable delay circuit 210, circuit 210 operates as a voltage controlled oscillator (VCO).

[0040] VCO 302 provides an internally generated clock signal VT, as discussed above with respect to VCO 202 of Figure 2. The frequency of clock signal VT is typically larger than the frequency of VIN. For example, the frequency of VT can be N times the frequency of VIN. Dividers 203 and 204 divide the frequency of VT by numbers N and M, respectively. Divider 203 divides the frequency of VT by N so that it equals the frequency of VIN. Divider 204 generates output signal VOUT.

[0041] Phase detector 201 compares the phase of VN with the phase of an input clock signal VIN. Phase detector 201 generates a phase detection signal that indicates the phase

difference between VIN and VN. Adjustable delay circuit 210 adjusts the phase of VT in response to the phase detection signal so that the phases of VIN and VN are aligned with each other, e.g., using a capacitor, as discussed above.

**[0042]** For example, if a rising edge of VN arrives before a rising edge of VIN, VCO 302 delays subsequent edges of VT. If a rising edge of VN arrives after a rising edge of VIN, VCO 302 causes subsequent edges of VT to occur earlier in time. When the rising edge of VIN aligns with the Nth rising edge of VT, circuit 300 is in equilibrium. Thus, in the first state of operation, circuit 300 operates much like a PLL.

**[0043]** The output signal of edge detector 315 goes HIGH one-half a period of VT before a rising edge of VN. When the output signal of edge-detector 315 is HIGH (and memory bit 320 is HIGH), VSEL is HIGH. VSEL remains HIGH for one period of VT. The second state of operation occurs when VSEL is HIGH.

**[0044]** When VSEL is HIGH, multiplexer 305 couples input clock signal VIN to an input of adjustable delay circuit 210. Feedback loop 312 is decoupled from the multiplexer 305 input of delay circuit 210. Therefore, circuit 302 does not act as a VCO. Instead, circuit 302 delays the edges of VIN to generate delay clock signal VT. Delay circuit 210 delays falling edges of VT by one-half a period of VT with respect to corresponding rising edges of VIN.

**[0045]** When VSEL is HIGH, a rising edge of VIN causes a falling edge of VT, because delay circuit 210 inverts VIN. The second state of operation is similar to the operation of a delay locked loop circuit.

**[0046]** In the second state of operation, frequency divided signal VN is compared with VIN to determine if there is a phase offset between the two signals. If a phase offset exists between VIN and VN, adjustable delay circuit 210 adjusts its delay time to the shift the phase of VT so that edges of VN and VIN are aligned.

**[0047]** The second state of operation lasts as long as VSEL is HIGH. Typically, VSEL is HIGH for one clock period of VT. However, in further embodiments of the present invention, the second state of operation can last for a longer or shorter period of time.

**[0048]** When the output signal of edge detector 315 transitions LOW again, VSEL also transitions LOW, feedback loop 312 converts circuit 302 back into a voltage controlled oscillator, and circuit 300 returns to the first state of operation.

**[0049]** The memory bit 320 can be pulled LOW to disable the second state of operation. When bit 320 is LOW, VSEL remains LOW even when the output of edge detector 315 goes HIGH. Circuit 302 remains configured as a VCO, and circuit 300 continuously operates in the first state of operation.

**[0050]** Figure 4 is a timing diagram that illustrates examples of signals generated by circuit 300 when it operates in hybrid PLL/DLL mode. Circuit 300 operates in hybrid PLL/DLL mode when memory bit 320 is HIGH. Figure 4 illustrates signals VIN, VT, VN, and VSEL. When VSEL is LOW, circuit 300 operates in the first state of operation. And when VSEL is HIGH, circuit 300 operates in the second state of operation.

**[0051]** When VSEL is LOW, circuit 302 operates as a voltage controlled oscillator. The VCO generates clock signal VT. Feedback loop 312 causes each HIGH pulse in VT to be related to the previous HIGH VT pulse. Each HIGH VT pulse is feed back through loop 312 to the input of delay circuit 210 to start the next HIGH VT pulse. The relationship between adjacent HIGH pulses in VT when VSEL is LOW is shown by arrows 405 in Figure 4. Because of this relationship, circuit 302 cannot change the phase of VT instantaneously to align with the phase of VIN when operating as a VCO in the first state of operation.

**[0052]** In the example of Figure 4, VSEL transitions HIGH to begin the second state of operation. The VSEL goes HIGH one-half of a VT cycle before the rising edge of VN. Arrows 401 from the falling edges of VT to the rising edges of VSEL in Figure 4 illustrate their relationship. The VSEL remains HIGH for one period of VT and then returns to LOW one-half a VT period after the rising edge of VN. This relationship is illustrated by arrows 402 in Figure 4.

**[0053]** When VSEL is HIGH, feedback loop 312 is decoupled from adjustable delay circuit 302, and multiplexer 305 provides VIN to the input of adjustable delay circuit 210. Thus, VT becomes a delayed version of VIN in the second state of operation. A rising edge in VIN that enters delay circuit 210 causes a corresponding falling edge in VT, because of the inversion in circuit 210. The rising edge of VT is delayed with respect to the corresponding falling edge in VIN by one-half a period of VT. The relationship between the edges of VIN and VT in the second state of operation are shown by arrows 403 in Figure 4.

**[0054]** Circuit 300 is typically designed to operate in the first state of operation most of the time as shown in Figure 4. In the first state of operation, the phase and frequency of VOUT cannot change instantaneously to match rapid changes in the phase or frequency of VIN.

Therefore, output signal VOUT of circuit 300 is stable even when the input signal VIN has a large jitter.

**[0055]** Circuit 300 can also use frequency dividers 203-204 to multiply the frequency of input signal VIN by a ratio N/M to generate the output signal VOUT. Thus, circuits of the present invention can provide many of the advantages of PLLs. According to further embodiments of the present invention, frequency dividers 203-204 can be removed. In these embodiments, phase detector 201 compares VIN directly to VOUT.

**[0056]** During the second state of operation, circuit 300 of the present invention can adjust the phase of output signal VOUT instantaneously to match changes in the phase and frequency of input signal VIN. Circuit 300 can lock and resynchronize more quickly to changes in the phase of input signal VIN than a standard PLL.

**[0057]** Also during the second state of operation of circuit 300, the jitter and drift in output signal VOUT matches the jitter and drift in input signal VIN. As a result, when the input signal VIN already has a low jitter, VOUT has less jitter and drift than a standard PLL output signal. Thus, circuits of the present invention also provide many of the advantages of DLLs.

**[0058]** Figure 5 is a timing diagram that illustrates examples of signals generated by circuit 300 when it operates in PLL mode. Circuit 300 operates in PLL mode when memory bit 320 is LOW. Figure 5 illustrates signals VIN, VT, VN, and VSEL.

**[0059]** VSEL is always LOW in PLL mode, and circuit 302 operates as a voltage controlled oscillator. Feedback loop 312 causes each HIGH pulse in VT to be related to the previous HIGH VT pulse. The relationship between adjacent HIGH pulses in VT in PLL mode is shown by arrows 501 in Figure 5.

**[0060]** PLLs and DLLs can be used in programmable integrated circuits to maintain a specific phase relationship between the master clock and the internal clock. Examples of programmable integrated circuits include programmable logic devices (PLDs), field programmable gate arrays (FPGAs), programmable logic arrays (PLAs), configurable PLDs, configurable gate arrays, etc.

**[0061]** Figure 6 is a simplified partial block diagram of an exemplary high-density PLD 600. Techniques of the present invention can be utilized in a PLD such as PLD 600. PLD 600 includes a two-dimensional array of programmable logic array blocks (or LABs) 602 that are interconnected by a network of column and row interconnects of varying length and

speed. LABs 602 include multiple (e.g., 10) logic elements (or LEs). An LE is a small unit of logic that provides for efficient implementation of user defined logic functions.

**[0062]** PLD 600 also includes a distributed memory structure including RAM blocks of varying sizes provided throughout the array. The RAM blocks include, for example, 512 bit blocks 604, 4K blocks 606 and a MegaBlock 608 providing 512K bits of RAM. These memory blocks may also include shift registers and FIFO buffers. PLD 600 further includes digital signal processing (DSP) blocks 610 that can implement, for example, multipliers with add or subtract features. I/O elements (IOEs) 612 located, in this example, around the periphery of the device support numerous single-ended and differential I/O standards. It is to be understood that PLD 600 is described herein for illustrative purposes only and that the present invention can be implemented in many different types of PLDs, FPGAs, and the like.

**[0063]** While PLDs of the type shown in Figure 6 provide many of the resources required to implement system level solutions, the present invention can also benefit systems wherein a PLD is one of several components. Figure 7 shows a block diagram of an exemplary digital system 700, within which the present invention may be embodied. System 700 can be a programmed digital computer system, digital signal processing system, specialized digital switching network, or other processing system. Moreover, such systems may be designed for a wide variety of applications such as telecommunications systems, automotive systems, control systems, consumer electronics, personal computers, Internet communications and networking, and others. Further, system 700 may be provided on a single board, on multiple boards, or within multiple enclosures.

**[0064]** System 700 includes a processing unit 702, a memory unit 704 and an I/O unit 706 interconnected together by one or more buses. According to this exemplary embodiment, a programmable logic device (PLD) 708 is embedded in processing unit 702. PLD 708 can serve many different purposes within the system in Figure 7. PLD 708 can, for example, be a logical building block of processing unit 702, supporting its internal and external operations. PLD 708 is programmed to implement the logical functions necessary to carry on its particular role in system operation. PLD 708 may be specially coupled to memory 704 through connection 710 and to I/O unit 706 through connection 712.

**[0065]** Processing unit 702 can direct data to an appropriate system component for processing or storage, execute a program stored in memory 704 or receive and transmit data via I/O unit 706, or other similar function. Processing unit 702 may be a central processing

unit (CPU), microprocessor, floating point coprocessor, graphics coprocessor, hardware controller, microcontroller, programmable logic device programmed for use as a controller, network controller, and the like.

**[0066]** Furthermore, in many embodiments, there is often no need for a CPU. For example, instead of a CPU, one or more PLDs 708 can control the logical operations of the system. In an embodiment, PLD 708 acts as a reconfigurable processor, which can be reprogrammed as needed to handle a particular computing task. Alternately, programmable logic device 708 can itself include an embedded microprocessor. Memory unit 704 can be a random access memory (RAM), read only memory (ROM), fixed or flexible disk media, PC Card flash disk memory, tape, or any other storage means, or any combination of these storage means.

**[0067]** While the present invention has been described herein with reference to particular embodiments thereof, a latitude of modification, various changes, and substitutions are intended in the present invention. In some instances, features of the invention can be employed without a corresponding use of other features, without departing from the scope of the invention as set forth. Therefore, many modifications may be made to adapt a particular configuration or method disclosed, without departing from the essential scope and spirit of the present invention. It is intended that the invention not be limited to the particular embodiment disclosed, but that the invention will include all embodiments and equivalents falling within the scope of the claims.